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(71)Applicant : SONY CORP

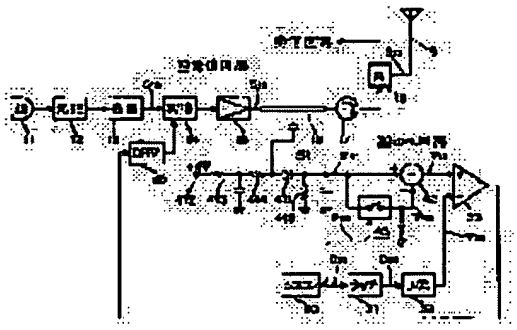
(72)Inventor : IIDA YUKIO
KITAKUBO KAZUTO
ISHIZUKA SEIJIRO
SATO HIDEAKI

(54) ENVELOPE DETECTION CIRCUIT

(57)Abstract:

PURPOSE: To eliminate temperature dependence in a detection output when an envelope of a burst high frequency signal is detected.

CONSTITUTION: An envelope detection circuit is provided with a detection circuit 41 detecting an envelope of a high frequency signal S13 obtained intermittently, with a sample-and-hold circuit 43 sampling and holding a detection output V41 of the detection circuit 41 when no high frequency signal S13 is obtained, and a subtractor circuit 42 subtracting the detection output 41 of the detection circuit 41 and an output V43 of the sample-and-hold circuit 43 to output a voltage V13 representing the envelope of the high frequency signal S13.



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[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] The detector circuit which carries out the envelope detector of the high frequency signal acquired intermittently,
The current regulator circuit which supplies constant current to the diode for detection which constitutes this detector circuit,
The sampling hold circuit which samples and holds the detection output of the above-mentioned detector circuit when the above-mentioned RF signal is not acquired,
The envelope detector which has the subtractor circuit which outputs the electrical potential difference which performs subtraction with the detection output of the above-mentioned detector circuit, and the output of the above-mentioned sampling hold circuit, and shows the envelope of the above-mentioned

high frequency signal.
[Claim 2] In the envelope detector of claim 1,
The A/D converter which carries out A/D conversion of the detection output of the above-mentioned detector circuit,
It has a D/A converter,
While the above-mentioned sampling hold circuit and the above-mentioned subtractor circuit perform each processing by digital processing,
The envelope detector which obtained the electrical potential difference which supplies the output of the above-mentioned subtractor circuit to the above-mentioned D/A converter, and shows the envelope of the above-mentioned high frequency signal.
[Claim 3] The gain control circuit to which the sending signal obtained intermittently is supplied,
Power amplification with which the output of this gain control circuit is supplied,
The detector circuit which carries out the envelope detector of a part of above-mentioned sending signal outputted from this power amplification,
The current regulator circuit which supplies constant current to the diode for detection which constitutes this detector circuit,
The sampling hold circuit which samples and holds the detection output of the above-mentioned detector circuit when the above-mentioned sending signal is not obtained,

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The envelope detector which it has in the subtractor circuit which outputs in the electrical potential difference which performs subtraction with the detector circuit which carries out the envelope detector of the high-frequency signal acquired intermittently, the sampling hold circuit which samples and holds the detection output of the above-mentioned detector circuit when the above-mentioned high-frequency signal is not acquired, the detection output of the above-mentioned detector circuit, and the output of the above-mentioned sampling hold circuit, and is shown in the envelope of the above-mentioned high-frequency signal.
[Claim 2] The envelope detector which obtained the electrical potential difference which supplies the output of the above-mentioned subtractor circuit to the above-mentioned D/A converter, and shows the envelope of the above-mentioned high frequency signal while it has the A/D converter which carries out A/D conversion of the detection output of the above-mentioned detector circuit, and a D/A converter in the envelope detector of claim 1 and the above-mentioned sampling hold circuit and the above-mentioned subtractor circuit perform each processing by digital processing.
[Claim 3] The envelope detector which supplied constant current to the diode for detection which constitutes the above-mentioned detector circuit in the envelope detector of claim 1 or claim 2.
[Claim 4] The gain control circuit to which the sending signal obtained intermittently is supplied, and the power amplification with which the output of this gain control circuit is supplied, The detector circuit which carries out the envelope detector of a part of above-mentioned sending signal outputted from this power amplification, The sampling hold circuit which samples and holds the detection output of the above-mentioned detector circuit when the above-mentioned sending signal is not obtained, The envelope detector which performs subtraction with the detection output of the above-mentioned detector circuit, and the output of the above-mentioned sampling hold circuit, has the subtractor circuit which outputs the electrical potential difference which shows the envelope of the above-mentioned high frequency signal, and controlled the gain of the above-mentioned gain control circuit based on the output of this subtractor circuit.

[Translation done.]